IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC. Plaintiff, v. **SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC.** Defendants.	)	Civil Action No. _____ JURY TRIAL DEMANDED

COMPLAINT

1. Plaintiff Netlist, Inc. ("Netlist"), by its undersigned counsel, brings this action against defendants Samsung Electronics Co., Ltd. ("SEC"), Samsung Electronics America, Inc. ("SEA"), and Samsung Semiconductor, Inc. ("SSI") (collectively, "Samsung" or "Defendants") for Samsung's infringement of U.S. Patent No. 12,308,087 ("the '087 Patent").

I. THE PARTIES

2. Plaintiff Netlist is a corporation organized and existing under the laws of the State of Delaware, having a principal place of business at 111 Academy Way, Suite 100, Irvine, CA 92617.

3. On information and belief, SEC is a corporation organized and existing under the laws of the Republic of Korea, with its principal place of business at 129 Samsung-ro, Yeongtong-gu, Suwon, Gyeonggi-Do, 443-742, Republic of Korea. On information and belief, SEC is the

worldwide parent corporation for SEA and SSI, and is responsible for the infringing activities identified in this Complaint. On information and belief, SEC's Device Solutions division is involved in the design, manufacture, use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below. On information and belief, SEC is also involved in the design, manufacture, and provision of products sold by SEA.

4. On information and belief, SEA is a corporation organized and existing under the laws of the State of New York. On information and belief, SEA, collectively with SEC, operates the Device Solutions division, which is involved in the design, manufacture, use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below. Defendant SEA maintains facilities at 6625 Excellence Way, Plano, Texas 75023. SEA may be served with process through its registered agent for service in Texas: CT Corporation System, 1999 Bryan Street, Suite 900, Dallas, Texas 75201. SEA is a wholly owned subsidiary of SEC.

5. On information and belief, SSI is a corporation organized and existing under the laws of the State of California. On information and belief, SSI, collectively with SEC, operates the Device Solutions division, which is involved in the design, manufacture, use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below. On information and belief, Defendant SSI maintains facilities at 6625 Excellence Way, Plano, Texas 75023. Defendant SSI may be served with process through its registered agent National Registered Agents, Inc., 1999 Bryan St., Ste. 900, Dallas, TX 75201-3136. On information and belief, SSI is a wholly owned subsidiary of SEA.

6. On information and belief, Defendants have used, sold, or offered to sell products and services, including the Accused Instrumentalities, in this judicial district.

II. JURISDICTION AND VENUE

7. Subject matter jurisdiction is based on 28 U.S.C. § 1338, in that this action arises under federal statute, the patent laws of the United States (35 U.S.C. §§ 1, *et seq.*).

8. Each Defendant is subject to this Court's personal jurisdiction consistent with the principles of due process and/or the Texas Long Arm Statute.

9. Personal jurisdiction exists generally over the Defendants because each Defendant has sufficient minimum contacts and/or has engaged in continuous and systematic activities in the forum as a result of business conducted within the State of Texas and the Eastern District of Texas. Personal jurisdiction also exists over each Defendant because each, directly or through subsidiaries, makes, uses, sells, offers for sale, imports, advertises, makes available, and/or markets products within the State of Texas and the Eastern District of Texas that infringe one or more claims of the Patent-in-Suit. Further, on information and belief, Defendants have placed or contributed to placing infringing products into the stream of commerce knowing or understanding that such products would be sold and used in the United States, including in this District.

10. Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b) and (c) and/or 1400(b). For example, SEC maintains a regular and established place of business in this judicial district at 6625 Excellence Way, Plano, Texas 75023 and has committed acts of infringement in this judicial district. As another example, SEA maintains a regular and established place of business in this judicial district at 6625 Excellence Way, Plano, Texas 75023 and has committed acts of infringement in this judicial district. Venue is also proper for SSI because it maintains a regular and established place of business in this judicial district at 6625 Excellence Way, Plano, Texas 75023 and has committed acts of infringement in this judicial district.

11. Defendants have not contested venue in this District. *See, e.g.*, Answer at ¶ 10, *Arbor Global Strategies LLC v. Samsung Elecs. Co., Ltd.*, No. 2:19-cv-333, Dkt. 43 (E.D. Tex.

Apr. 27, 2020); Answer at ¶ 29, *Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.*, No. 2:19-cv-347, Dkt. 14 (E.D. Tex. Feb. 12, 2020). Nor have Defendants contested venue in any of the prior actions between the parties in this district. *See Netlist, Inc. v. Samsung Elecs. Co. Ltd.*, No. 2:21-cv-463 (E.D. Tex.) ("*Samsung I*"), *Netlist, Inc. v. Samsung Elecs. Co. Ltd.*, No. 2:21-cv-293 (E.D. Tex.) ("*Samsung II*").

III. FACTUAL ALLEGATIONS

A. Background

12. Since its founding in 2000, Netlist has been a leading innovator in high-performance memory module technologies. Netlist designs and manufactures a wide variety of high-performance products for the cloud computing, virtualization and high-performance computing markets. Netlist's technology enables users to derive useful information from vast amounts of data in a shorter period of time. These capabilities will become increasingly valuable as the volume of data continues to dramatically increase. Netlist has secured multiple jury verdicts confirming the commercial success of its inventions. For example, in 2023, a jury in the Eastern District of Texas found that Samsung willfully infringed five Netlist patents and awarded Netlist $303.15 million in damages. *See Netlist, Inc. v. Samsung Elecs. Co., Ltd.*, No. 2:21-cv-463, Dkt. 479. As another example, in 2024, a jury in the Eastern District of Texas awarded Netlist $445 million in damages against Micron, another dominant memory module manufacturer. *See Netlist, Inc. v. Micron Technology Texas, LLC*, No. 2:22-cv-294, Dkt. 135. And in November 2024, a jury in the Eastern District of Texas found that Samsung willfully infringed three other Netlist patents and awarded Netlist $118 million in damages. *See Netlist, Inc. v. Samsung Elecs. Co., Ltd.*, No. 2:22-cv-293, Dkt. 847.

13. Netlist has a long history of being the first to market with disruptive new products such as the first load-reduced dual in-line memory module ("LR-DIMM"), HyperCloud®, based

on Netlist's distributed buffer architecture later adopted by the industry for DDR4 LRDIMM. Netlist was also the first to bring NAND flash to the memory channel with its NVvault® NVDIMM. Netlist's pioneering NVDIMM products utilized the same on-module power management technology found on newer-generation DDR5 DIMMs. These innovative products built on Netlist's early pioneering work in areas such as embedding passives into printed circuit boards to free up board real estate, doubling densities via quad-rank double data rate (DDR) technology, and other off-chip technology advances that result in improved performance and lower costs compared to conventional memory.

14. In many commercial products, a memory module is a printed circuit board that contains, among other components, a plurality of individual memory devices (such as DRAMs). The memory devices are typically arranged in "ranks," which are accessible by a processor or memory controller of the host system. A memory module is typically installed into a memory slot on a computer motherboard.

15. Memory modules are designed for, among other things, use in servers such as those supporting cloud-based computing and other data-intensive applications. Memory modules are typically characterized by, among other things, the generation of DRAM on the module (*e.g.*, DDR5, DDR4, DDR3) and the type of module (*e.g.*, RDIMM, LRDIMM).

B. The '087 Patent

16. The '087 Patent is entitled "Memory Package Having Stacked Array Dies and Reduced Driver Load," and was filed on March 14, 2022 and assigned to Netlist, Inc. The '087 Patent issued on May 20, 2025 (Ex. 1) and claims priority to, among others, U.S. Application No. 13/288,850, filed Nov. 3, 2011, and U.S. Provisional No. 61/409,893, filed November 3, 2010.

17. Claim 1 of the '087 Patent provides:

[1pre] A dynamic random access memory (DRAM) package, comprising:

[1a] stacked DRAM dies including at least a first plurality of DRAM dies and a second plurality of DRAM dies, each DRAM die of the stacked DRAM dies including C/A ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;

[1b] terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals, wherein the DRAM package is configured to output first data signals in response to a first set of C/A signals associated with a memory read operation and to receive second data signals in response to a second set of C/A signals associated with a memory write operation;

[1c] die interconnects including C/A interconnects and data interconnects, the C/A interconnects including at least first C/A interconnects and second C/A interconnects, the first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including at least first data interconnects and second data interconnects, the first data interconnects configured to conduct the first data signals and the second data signals, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies and configured to conduct signals to and/or from the one or more DRAM dies in the stacked DRAM dies through the one or more TSVs;

[1d] a control die coupled between the terminals and the stacked DRAM dies, the control die including conduits, the conduits including C/A conduits and data conduits, the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects and second C/A conduits coupled to respective ones of the second C/A interconnects, the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects;

[1e] wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the second plurality of DRAM dies;

[1f] wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of

DRAM dies and not in electrical communication with any C/A port on any of the first plurality of DRAM dies;

[1g] wherein a first data interconnect of the first data interconnects is in electrically communication with corresponding data ports on the first plurality of DRAM dies and not in electrical communication with any data port on any of the second plurality of DRAM dies, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one TSV in at least one DRAM die of the second plurality of DRAM dies, wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die;

[1h] wherein a second data interconnect of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;

[1i] wherein a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal;

[1j] wherein the control die further includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal;

[1k] wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies;

[1l] wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured conduct any signal from any of the stacked DRAM dies to the control die;

[1m] wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and is not configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects;

[1n] wherein the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects; and

[1o] wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects.

C. Samsung's Infringing Activities

18. Samsung is a global technology company and one of the largest manufacturers of semiconductor memory products such as DRAM, NAND Flash, and MCP (Multi-Chip Package) such as high-bandwidth memories ("HBM"). Samsung develops, manufactures, sells, offers to sell, and imports into the United States memory components and memory modules designed for, among other things, use in servers such as those supporting cloud-based computing and other data-intensive applications.

19. Samsung and Netlist were initially partners under a 2015 Joint Development and License Agreement ("JDLA"), which granted Samsung a 5-year paid-up license to Netlist's patents "having an effective first filing date on or prior to" November 12, 2020. *See Netlist Inc. v. Samsung Elecs. Co., Ltd.*, No. 20-cv-993, Dkt. 186 at 20-21 (C.D. Cal. Oct. 14, 2021). On information and belief, Samsung used Netlist's technologies to develop products both in the mature markets such as DDR4 memory modules and the emerging market for new generations of DRAM technologies, including DDR5 and HBMs. Under the JDLA, Samsung was obligated to supply Netlist certain memory products at competitive prices. Samsung, however, did not honor its promises and

repeatedly failed to fulfill Netlist's product orders. As a result, Netlist terminated the JDLA on July 15, 2020, which termination was found effective on summary judgment by a federal district court in the Central District of California on October 14, 2021. *Id.*

20. Samsung appealed this decision, and the Ninth Circuit partially reversed the summary judgment ruling. Following remand, the contract action in C.D. Cal. proceeded to a jury trial. On May 17, 2024, the jury returned a verdict finding that Netlist's interpretation of the JDLA's supply provision was correct, and Samsung's breach of that provision was material. On December 26, 2024, the Court granted Samsung's motion for a new trial, and a new trial was held on March 18-21, 2025. On March 24, 2025, the jury returned a verdict for Netlist. As a result of this jury verdict, Samsung's license to Netlist's patents was terminated on July 15, 2020.

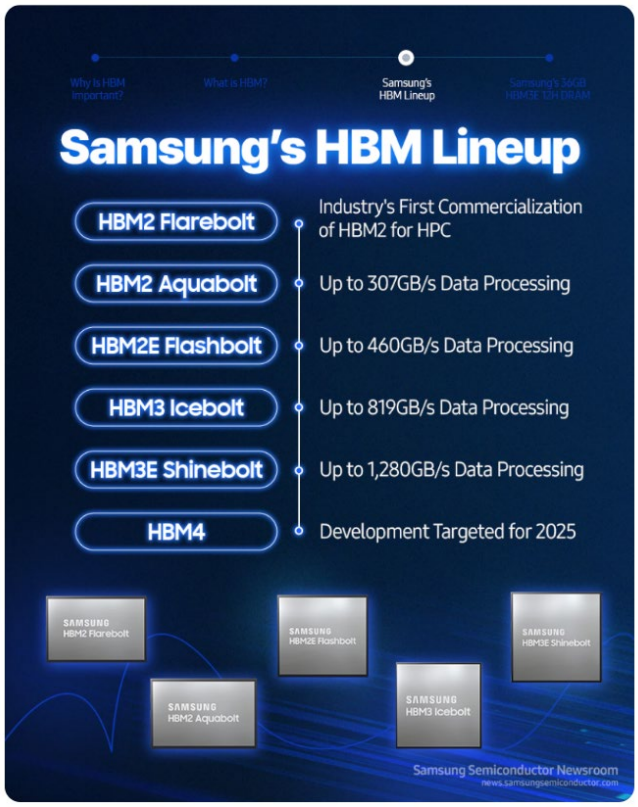
21. In April 2023, a jury in the Eastern District of Texas found that Samsung willfully infringed five Netlist patents and awarded Netlist $303.15 million in damages, including $122,775,000 for U.S. Patent Nos. 8,787,060 and 9,318,160 asserted against Samsung's HBM products. And in November 2024, a jury found that Samsung willfully infringed three different Netlist patents and awarded Netlist $118 million in damages. *See Netlist, Inc. v. Samsung Elecs. Co., Ltd.*, No. 2:22-cv-293, Dkt. 847.

D. High Bandwidth Memory ("HBM")

22. HBM is a type of high-speed computer memory technology that relies in part on vertically-stacked memory dies and differs from the DDR4 or DDR5 DIMM formats described in the paragraphs above. Samsung is a major supplier of HBM. Samsung itself confirms that its HBM products are "optimized for high-performance computing (HPC), and offer the performance needed to power next-generation technologies, such as artificial intelligence (AI)." Ex. 2 at 1.

23. The Accused HBM Products include, without limitation, any Samsung HBM2, HBM2E, HMB3, HBM3E and newer products (e.g., HBM4) made, sold, used, offered for sale,

and/or imported into the United States by Samsung. By way of non-limiting example, the accused HBM products include Samsung products marketed as "Aquabolt," "Flashbolt," or "Icebolt." The Accused HBM Products further include Samsung's HBM3e products (also known as "Shinebolt"), which it describes as "the highest-capacity HBM product to date." Ex. 3 at 1. Samsung launched HBM3e in February 2024, and is in the process of qualifying HBM3e with its customers[1]: "A version of Samsung Electronics' (005930.KS), fifth-generation high bandwidth memory (HBM) chips, or HBM3E, has passed Nvidia's (NVDA.O) tests for use in its artificial intelligence (AI) processors."



Ex. 4 at 2.

[1] https://www.reuters.com/technology/artificial-intelligence/samsungs-8-layer-hbm3e-chips-clear-nvidias-tests-use-sources-say-2024-08-06/

24. On information and belief, the Accused HBM Products are compliant with the applicable memory standards promulgated by the Joint Electron Device Engineering Council ("JEDEC").

25. Samsung's HBM products are comprised of stacked dies interconnected by through silicon vias ("TSVs"). Samsung touts the performance benefits enabled by the ability to vertically stack a large number of dies within a single package. *See, e.g.*, Ex. 4 at 2 ("HBM is the fastest DRAM in the market with highest-bandwidth among all memory solutions. By vertically stacking thin DRAM chips, HBM achieves the performance and capacity demanded by large AI models.").

Stacking the Chips and Packaging
The strategic stacking of 12 layers of 24Gb DRAM chips using Through-Silicon Via (TSV) technology gives the HBM3E astounding bandwidth and an industry-leading 36GB of capacity per layer. This scheme improves capacity by 50% over its 12-layer HBM3 predecessor. The HBM3E and HBM3 chip sizes are compatible with each other, allowing easy transfer of hardware layouts from HBM3 to HBM3E.

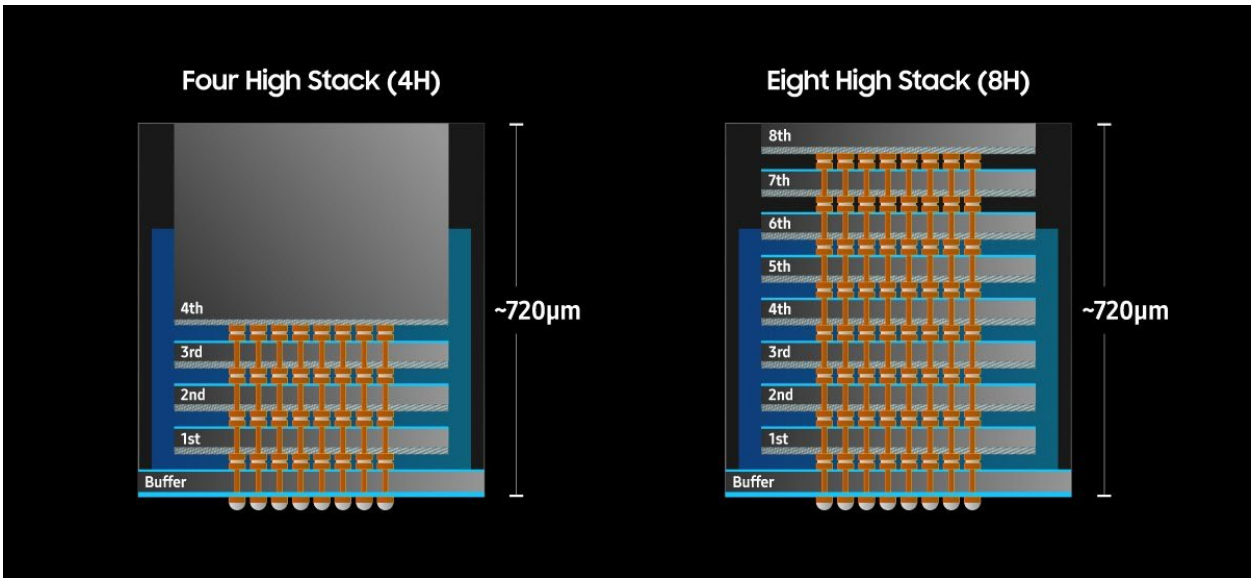
Ex. 5 at 1.

IV. FIRST CLAIM FOR RELIEF

26. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

27. On information and belief, Defendants directly infringed and are currently infringing at least one of the approved claims of the '087 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the Accused HBM Products, and other products with materially the same structure in relevant part. For example, and as shown below, the Accused HBM Products and other products with materially the same structure and operating mechanisms in relevant part infringe at least Claim 1 of the '087 Patent.

28. To the extent the preamble is limiting, the Accused HBM Products are a DRAM package. Additionally, as shown below, the Accused HBM Products each include stacked DRAM dies (*e.g.*, 8, 12, or 16 DRAM dies) including at least a first plurality and second plurality of DRAM dies, with each DRAM die of the stacked DRAM dies including C/A ports, data ports, and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells. *See, e.g.*, Ex. 6 at 2-3 (reproduced below); Ex. 7 at 1 ("With 12 stacks of startlingly fast DRAM, HBM3 Icebolt is high-bandwidth memory at its fastest, most efficient, and highest capacity."); Ex. 8 (Samsung announcing manufacturing of 16H HBM).



29. The Accused HBM Products also include terminals with command and/or address (C/A) terminals and data terminals, via which the memory package communicates, e.g., control/address signals and data signals in response to the C/A signals, respectively. For example, the DRAM package is configured to output first data signals in response to a first set of C/A signals associated with a memory read operation, and to receive second data signals in response to a second set of C/A signals associated with a memory write operation. To illustrate, JEDEC Standard No. 238A provides the following Command Truth Table listing the command and/or address signals associated with a memory read operation and memory write operation:

6.3.1 Command Truth Tables (cont'd)

Table 31 — Column Commands Truth Table

Command [4]	Symbol	Clock Cycle	C0	C1	C2	C3	C4	C5	C6	C7	Notes
Column No Operation	CNOP	R	H	H	H	V	V	V	V	V	1, 2, 3
		F	V	V	V	V	V	V	V	V	
Read	RD	R	H	L	H	L	PC	SID0 / V	SID1 / V	BA0	1, 2, 3, 5, 6, 7
		F	BA1	BA2	BA3	CA0	CA1	CA2	CA3	CA4	
Read w/ AP	RDA	R	H	L	H	H	PC	SID0 / V	SID1 / V	BA0	1, 2, 3, 5, 6, 7
		F	BA1	BA2	BA3	CA0	CA1	CA2	CA3	CA4	
Write	WR	R	H	L	L	L	PC	SID0 / V	SID1 / V	BA0	1, 2, 3, 5, 6
		F	BA1	BA2	BA3	CA0	CA1	CA2	CA3	CA4	
Write w/ AP	WRA	R	H	L	L	H	PC	SID0 / V	SID1 / V	BA0	1, 2, 3, 5, 6
		F	BA1	BA2	BA3	CA0	CA1	CA2	CA3	CA4	
Mode Register Set	MRS	R	L	L	L	MA4	OP5	OP6	OP7	MA0	1, 3, 8, 9
		F	MA1	MA2	MA3	OP0	OP1	OP2	OP3	OP4	

NOTE 1 BA = Bank Address; CA = Column Address; PC = Pseudo Channel 0 or 1; SID = Stack ID; MA = Mode Register Address; V = Valid Signal (either H or L, but not floating).

NOTE 2 C[7:0] must be driven to a valid signal level even if a stack ID address (SID) is not defined for a specific density, or if parity is disabled in the mode register. APAR must be driven to a valid signal level even if CA parity is disabled in MR0 OP6. C[7:0] are Don't Care when the device is in power-down or self refresh.

NOTE 3 Parity is evaluated on all pins if CA parity is enabled in MR0 OP6.

NOTE 4 All other command encodings not shown in the table are reserved for future use.

NOTE 5 PC = 0 selects pseudo channel 0 (PC0), and PC = 1 selects pseudo channel 1 (PC1). The pseudo channel not selected by PC performs a CNOP.

NOTE 6 The SID bits act as bank address bits in conjunction with READ and WRITE commands, and related timing diagrams shall be interpreted accordingly. All other column commands do not use SID. Refer to the channel addressing table for HBM3 configurations using SID.

NOTE 7 HBM3 configurations using the SID specify a timing parameter t_{CCDR} for consecutive READs to different SID. Vendor datasheets should be consulted for details.

NOTE 8 All mode registers are write-only by default using the MRS command.

NOTE 9 Refer to the HBM3 Mode Register Overview table for MA4 of MRS.

Ex. 9 at 36.

30. The Accused HBM Products further include die interconnects including C/A interconnects and data interconnects, the C/A interconnects including at least first C/A interconnects and second C/A interconnects, the first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including at least first data interconnects and second data interconnects, the first data interconnects configured to conduct the first data signals and the second data signals, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies and configured to conduct signals to and/or from the one or more DRAM dies in the stacked

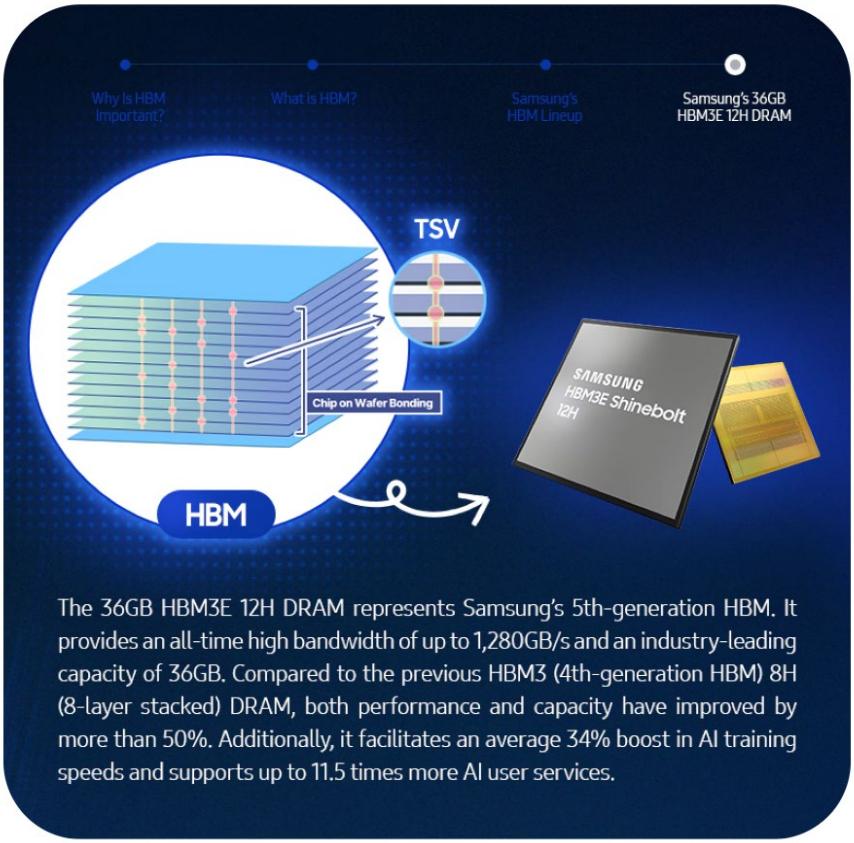
DRAM dies through the one or more TSVs. *See, e.g.*, Ex. 5 at 1 ("The strategic stacking of 12 layers of 24Gb DRAM chips using Through-Silicon Via (TSV) technology gives the HBM3E astounding bandwidth and an industry-leading 36GB of capacity per layer. This scheme improves capacity by 50% over its 12-layer HBM3 predecessor."); Ex. 6 at 2 ("HBM employs stacks of vertically interconnected DRAM chips, supports 1,024 I/Os and implements Through Silicon Via (TSV) technology, where connections between die are achieved through thousands of copper-filled holes functioning as wires with alternating layers of external microbumps.").

31. As shown above, the Accused HBM Products also include a control die (also known as a "buffer die" or "logic die") coupled between the terminals and the stacked DRAM dies. The control die includes conduits including C/A conduits and data conduits, the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects and second C/A conduits coupled to respective ones of the second C/A interconnects, the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects.

32. The Accused HBM Products also have C/A interconnects in the claimed configuration. For example, a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not with any C/A port on any of the second plurality of DRAM dies. Similarly, a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not with any C/A port on any of the first plurality of DRAM dies.

33. The Accused HBM Products also have data interconnects in the claimed configuration. For example, a first data interconnect of the first data interconnects is in electrical communication with corresponding data ports on the first plurality of DRAM dies and not with

any data port on any of the second plurality of DRAM dies. Further, each of the first data interconnects includes a first respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one TSV in at least one DRAM die of the second plurality of DRAM dies, wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die. Similarly, a second data interconnect of the second data interconnects is in electrical communication with data ports on the second plurality of DRAM dies and not with any data port on any of the first plurality of DRAM die. For example, as depicted below, some TSVs appear to only electrically interconnect to some of the dies in the stack, while others may electrically bypass certain groups of dies.



Ex. 4 at 2.

34. Additionally, the data conduits in the control die include a first conduit of the first data conduits coupled between the first data interconnect and a first data terminal of the data terminals (e.g., one or more data terminals), and a second conduit of the second data conduits coupled between the second data interconnect and the first data terminal (e.g., one or more data terminals). The control die also includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal (e.g., as shown above in the Command Truth Table of JESD 238A, Ex. 9 at 36).

35. The Accused HBM Products further include first and second unidirectional die interconnects, for example, respective TSVs associated with unidirectional differential data strobes RDQS_t/RDQS_c and WDQS_t/WDQS_c. *See, e.g.*, JESD 238A, Ex. 9 at 1 ("Data referenced to unidirectional differential data strobes RDQS_t/RDQS_c and WDQS_t/WDQS_c."); *id.* at 26-27 (reproduced below). For example, the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects (*e.g.*, RDQS_t/RDQS_c in response to the first set of C/A signals) and is not configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects. As further example, the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects (e.g., WDQS_t/WDQS_c in response to the second set of C/A signals) and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects.

6 Operation

6.1 HBM3 Clocking Overview

The HBM device captures commands and addresses on the row and column buses using a differential clock CK_t/CK_c. Both buses operate at double data rate (DDR).

The HBM device has uni-directional differential Write strobes (WDQS_t/WDQS_c) and Read strobes (RDQS_t/RDQS_c) per 32DQ(DWORD). The data bus operates at double data rate (DDR).

HBM3 utilizes two types of clock with different frequencies. The strobe frequency is twice the frequency of the command clock, requiring an HBM3 to have reset-type clock-divider in the WDQS clock tree (Figure 10). By dividing the WDQS, the operation speed of DRAM internal circuits in WDQS domain is reduced to half. The direction of the internal WDQS/2 transition may vary depending on vendor's choice. Command clock and WDQS are generated from the same PLL and RDQS clock is generated from WDQS. WDQS internal divider is initialized to be a pre-defined internal divider state after Self Refresh exit or Power-up or Power down exit sequence. The sum of preamble and postamble for both READ and WRITE operation is required to be an even number so that the internal divider's state, phase of internal WDQS/2, is maintained. Therefore, HBM3 WDQS does not require a specific sync operation before READ and WRITE operations. WDQS starts toggling before starting WRITE or READ operations for reducing ISI. During inactivity, WDQS/ RDQS are required to be static (WDQS/RDQS_t is Low, WDQS/RDQS_c is High). When WRITE training for unmatched DQ/DQS path, DQ should be shifted to align phase to the point where CK and WDQS are in sync.

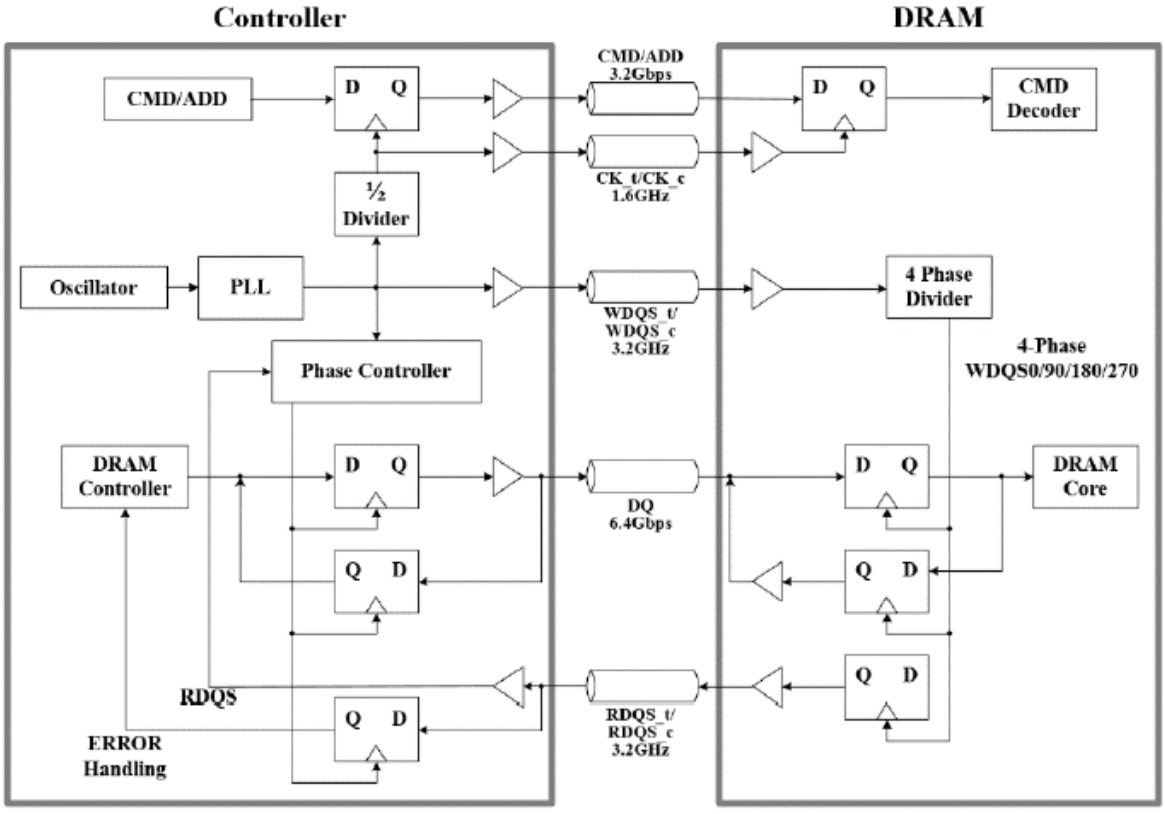


Figure 10 — High Level Block Diagram Example of Clocking Scheme

V. DEMAND FOR JURY TRIAL

36. Pursuant to Federal Rule of Civil Procedure 38(b), Netlist hereby demands a trial by jury on all issues triable to a jury.

VI. PRAYER FOR RELIEF

WHEREFORE, Netlist respectfully requests that this Court enter judgment in its favor ordering, finding, declaring, and/or awarding Netlist relief as follows:

A. that Samsung infringes the Patent-in-Suit;

B. all equitable relief the Court deems just and proper as a result of Samsung's infringement;

C. an award of damages resulting from Samsung's acts of infringement in accordance with 35 U.S.C. § 284;

D. that Samsung's infringement of the Patent-in-Suit is willful;

E. enhanced damages pursuant to 35 U.S.C. § 284;

F. that this is an exceptional case and awarding Netlist its reasonable attorneys' fees pursuant to 35 U.S.C. § 285;

G. an accounting for acts of infringement and supplemental damages, without limitation, prejudgment and post-judgment interest; and

H. such other equitable relief which may be requested and to which Netlist is entitled.

Dated: May 19, 2025

Respectfully submitted,

/s/ Jennifer L. Truelove

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